IN THE CLAIMS:

Please cancel claims 1-10 and 12-13 and amend the claims as follows:

1-10 (Canceled)

11. (Currently Amended) A memory cell formed on a substrate, comprising:
a trench capacitor; and
a select transistor, comprising:
a diffusion region forming a source/drain electrode of the select transistor;
a bit-line contact formed in an insulator layer and comprising a filling comprising at least one of a metal and a metal alloy, wherein the bit-line contact connects the source/drain [[region]] electrode to an associated bit line; and
a doped region formed in the source/drain electrode to contact ~~between the substrate and~~ the filling of the bit-line contact, the doped region comprising a locally limited electrically conductive contact layer which is formed underneath the bit-line contact in the diffusion region and which has a relatively reduced lateral migration underneath the insulator layer adjoining the bit-line contact.

12. (Canceled)

13. (Canceled)

14. (Original) The memory cell of claim 11, wherein the select transistor is at least partially disposed in the substrate and the trench capacitor is completely disposed in the semiconductor substrate.

15. (Original) The memory cell of claim 11, wherein the bit-line contact comprises at least one of tungsten, aluminum and copper.

16. (Currently Amended) The memory cell of claim 11, wherein the memory cell is part of a memory cell arrangement comprising peripheral contacts [[are]] formed in a same structure plane and comprising a filling substantially similar to that of the bit-line contact.

17. (Original) The memory cell of claim 11, the bit-line contact further comprising a liner layer formed between the substrate and the filling of the bit-line contact.

18. (Original) The memory cell of claim 17, wherein the liner layer comprises at least one of Ti and Ti/TiN.

19. (Currently Amended) A memory cell formed on a substrate, comprising:
a trench capacitor; and
a select transistor, comprising:
a diffusion region forming a source/drain electrode of the select transistor;
a bit-line contact formed in an insulator layer and comprising a filling comprising at least one of a metal and a metal alloy, wherein the bit-line contact connects the source/drain [[region]] electrode to an associated bit line;
a doped region formed [[on]] in the source/drain [[region]] electrode between the substrate and the filling of the bit-line contact, the doped region comprising a locally limited electrically conductive contact layer which is formed underneath the bit-line contact in the diffusion region and which has a relatively reduced lateral migration underneath the insulator layer adjoining the bit-line contact; and
an annealed region formed as a result of an anneal process performed during fabrication of the bit-line contact.

20. (Original) The memory cell of claim 19, wherein the annealed region includes a damaged region damaged during a doping processed performed to form the doped region.

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21. (Original) The memory cell of claim 19, wherein the annealed region includes at least a portion of the doped region.

22. (Original) The memory cell of claim 19, the bit-line contact further comprising a liner layer formed between the substrate and the filling of the bit-line contact.

Please add the following new claims:

23. (New) The memory cell of claim 22, wherein the liner layer comprises at least one of Ti and Ti/TiN.

24. (New) The memory cell of claim 19, wherein another source/drain electrode of the select transistor is connected to an electrode of the trench capacitor which is completely disposed in the substrate.

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